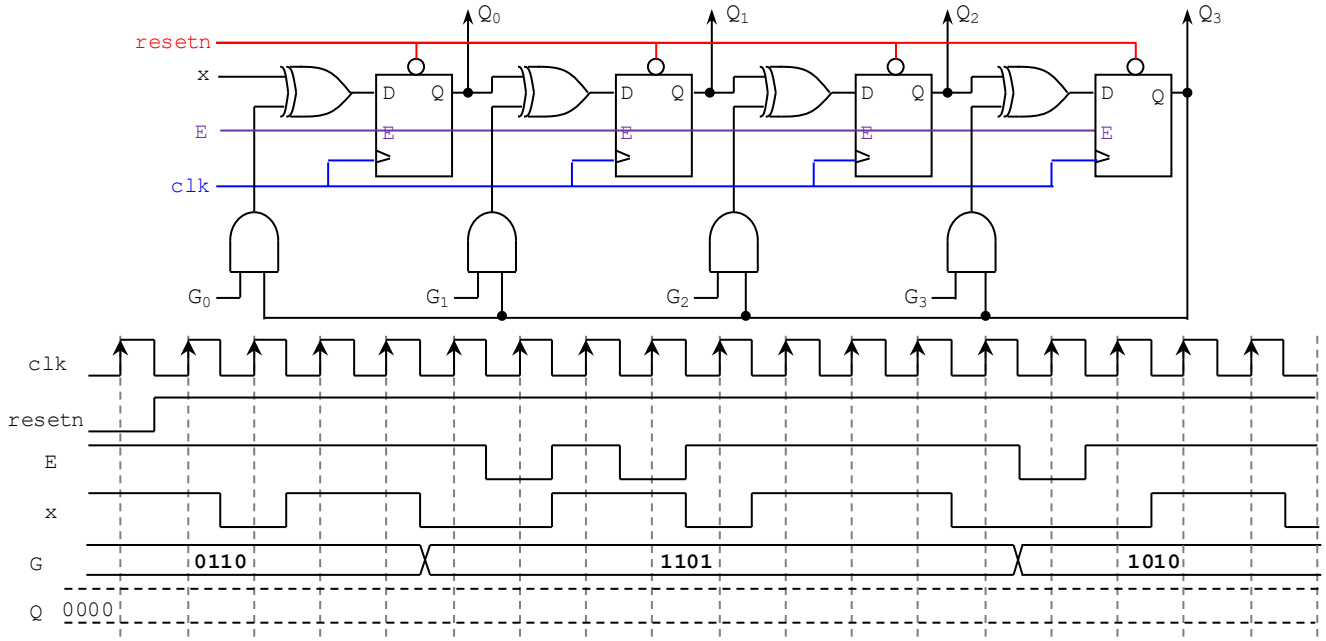
Homework 4

(Due date: November 16th @ 11:59 pm)

Presentation and clarity are very important! Show your procedure!

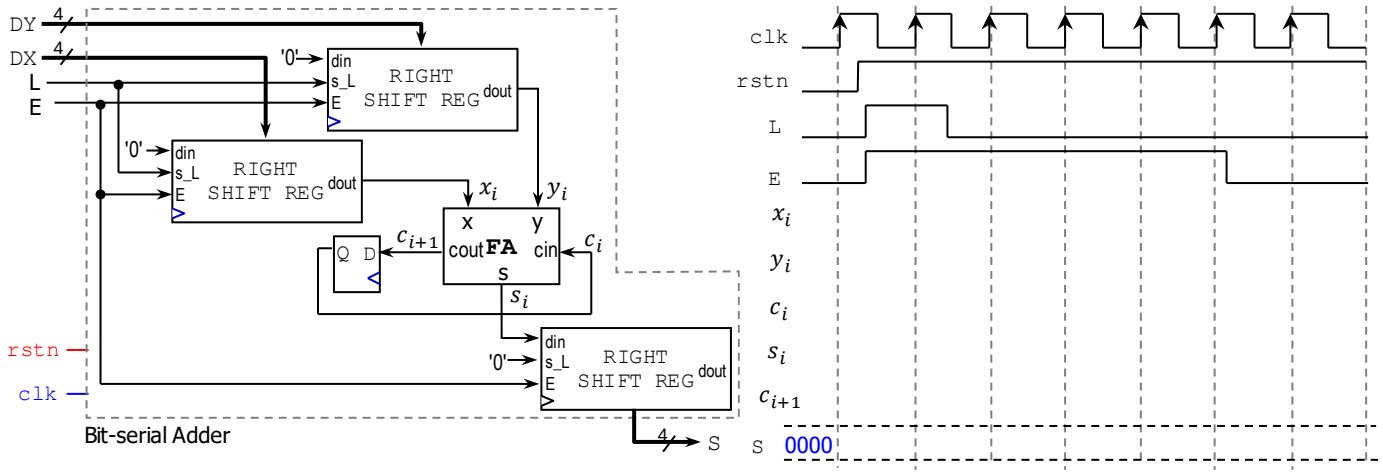
PROBLEM 1 (14 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0$, $Q = Q_3Q_2Q_1Q_0$

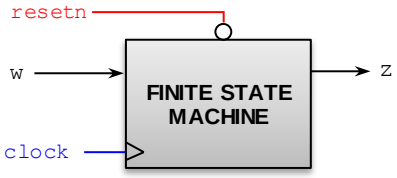


PROBLEM 2 (18 PTS)

- Complete the timing diagram of the following bit-serial adder. DX=1011, DY=1010. (8 pts)



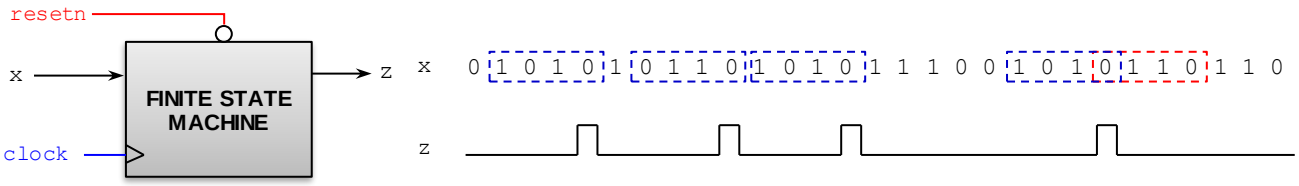
- The following FSM has 4 states, one input w and one output z. (10 pts)
  - ✓ The excitation equations are given by:
    - $Q_1(t+1) \leftarrow Q_0(t)$
    - $Q_0(t+1) \leftarrow \overline{Q_1(t) \oplus w}$
  - ✓ The output equation is given by: $z = Q_1(t) \oplus \overline{Q_0(t)} \oplus w$



  - ✓ Is it a Mealy or Moore Machine? Why?
  - ✓ Provide the State Diagram (any representation) and the Excitation Table. (6 pts)
  - ✓ Sketch the Finite State Machine circuit. (3 pts)

PROBLEM 3 (21 PTS)

- Sequence detector: This FSM has to generate $z = 1$ when it detects the sequence 1010 or 0110. Once the sequence is detected, the circuit looks for a new sequence. Note that once we start detecting a sequence, we prioritize the sequence that we have over the other (e.g.: last sequence inside a dotted red rectangle is not considered).

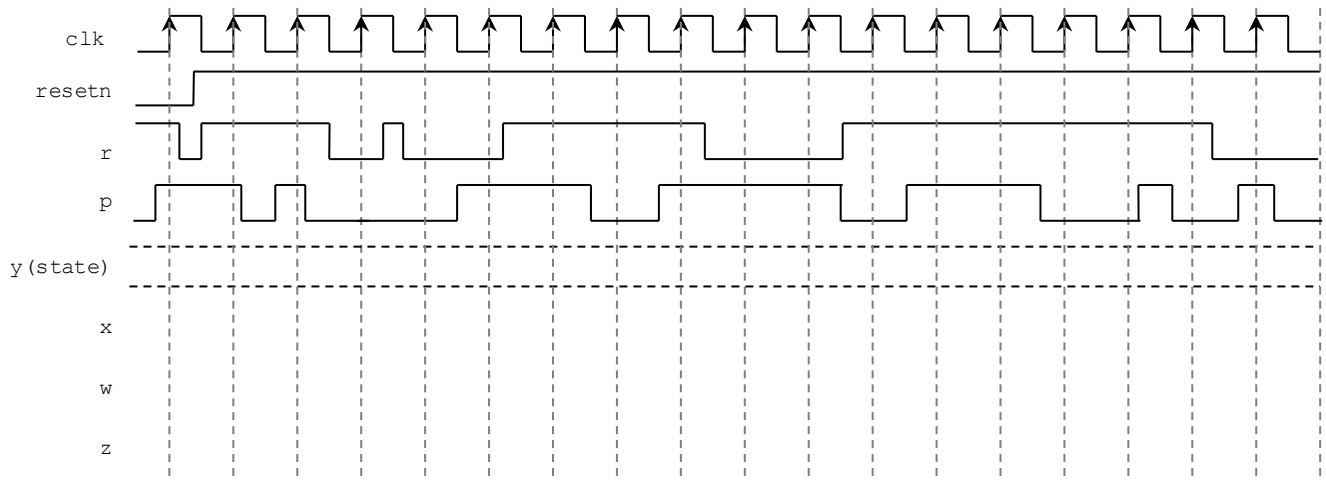


- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit. (14 pts)
- Provide the excitation equations and the Boolean equation for z (simplify your circuit: K-maps or Quine-McCluskey) (4 pts)
- Sketch the circuit. Is this a Mealy or a Moore machine? Why? (3 pts)

PROBLEM 4 (15 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;

architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;

begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '0' then y <= S2;
            else
               if p = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if p = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if p = '1' then y <= S3; else y <= S2; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '1' then z <= '1'; end if;

         when S2 => if r = '0' then x <= '1'; end if;
                    if p = '0' then w <= '1'; end if;

         when S3 => x <= '1';
      end case;
  end process;
end behavioral;
```



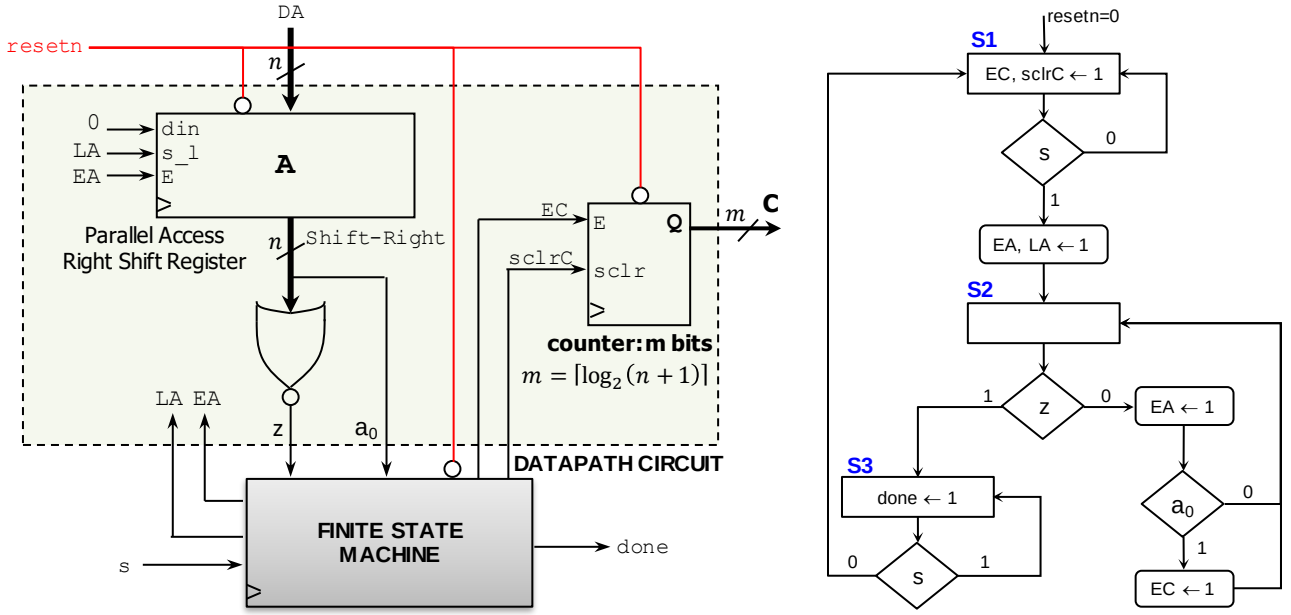
PROBLEM 5 (17 PTS)

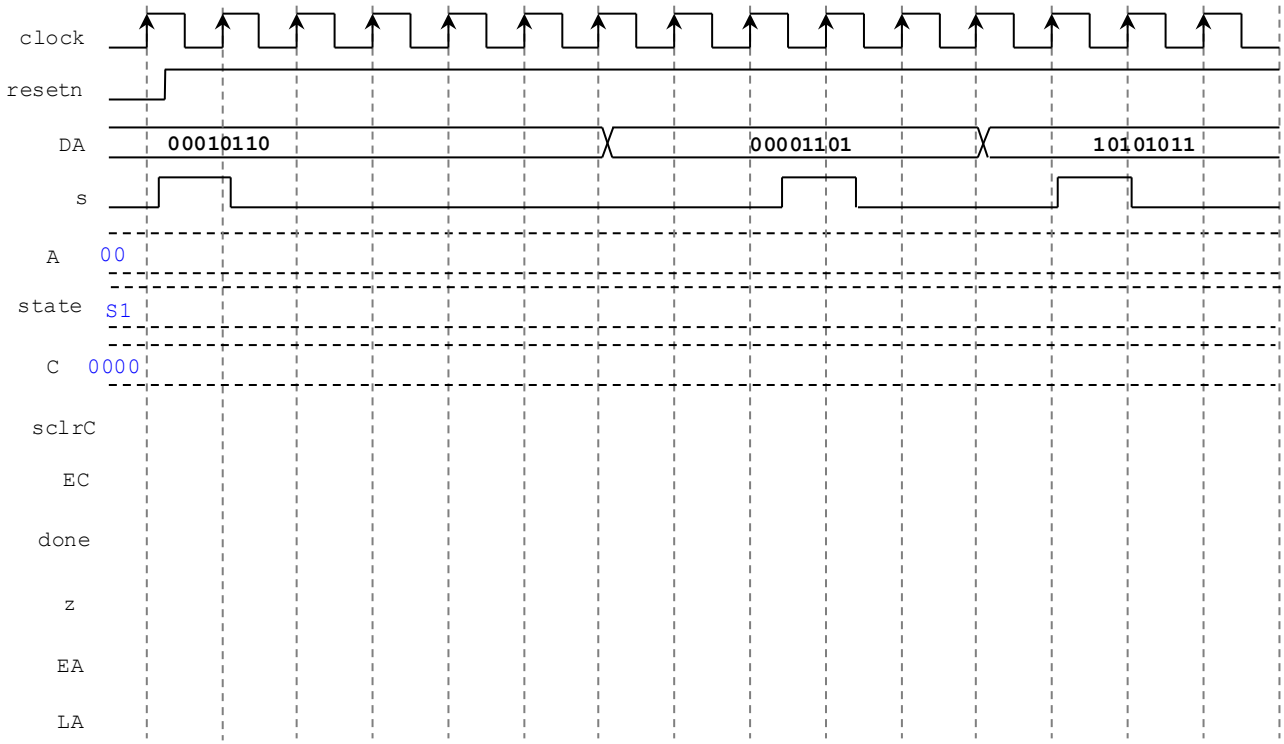
- "Counting 1's" Circuit: It counts the number of bits in register A that has the value of '1'. Example: for $n = 8$: if $A = 00110010$, then $C = 0011$. The circuit includes an FSM and a datapath circuit. The behavior of the generic components is as follows:

m-bit counter (modulo-n+1): If E=0, the count stays.	n-bit Parallel access shift register: If E=0, the output is kept.

`if E = 1 then`
`  if sclr = 1 then`
`  Q ← 0`
`  else`
`  Q ← Q+1`
`  end if;`
`end if;`
	`if E = 1 then`
	`  if s_l = '1' then`
	`  Q ← D`
	`  else`
	`  Q ← shift in 'din' (to the right)`
	`  end if;`
	`end if;`

- Complete the timing diagram where $n = 8, m = 4$. A is represented in hexadecimal format, while C is in binary format.





PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than 3 pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about the design and its components. You **MUST** use the provided template (`Final Project - Report Template.docx`).